

REMARKS

Reconsideration and allowance of this application are respectfully requested. Claims 1-2 and 21-33 are presented for the Examiner's reconsideration.

In the Office Action, the Examiner rejected claims 1-2, 21-22, 24, 26-30 and 32 under 35 U.S.C. § 103(a) as being unpatentable over *Yamazaki* (U.S. Patent No. 5,306,940) in view of *Kinney* (U.S. Patent No. 5,179,038) and *Kagaya* (U.S. Patent No. 5,523,593). It is submitted, however, that the claims are patentably distinguishable over the references.

The *Yamazaki* patent is directed to an element isolation region of a semiconductor device. *Yamazaki* shows, in Figs. 1A-1D, a U-shaped trench 212 that is filled with a polysilicon film 252. The top of the trench is covered with a field oxide film 210b. (See col. 8, line 34 to col. 9, line 14). The patent also shows, in Figs. 4A-4B, a U-shaped trench 112 in which the sidewalls and the bottom of a lower portion are lined with a silicon oxide film 113, and the rest of the lower portion is filled with a BPSG film 115c. The upper part of the trench is filled with a silicon oxide film 116a. (See col. 10, line 64 to col. 11, line 59).

The *Kinney* patent is concerned with forming isolation trenches in a CMOS integrated circuit. *Kinney* shows, in Figs. 4-7, isolation trenches 24, 70 in which the sidewalls of the entire trench are lined with a thin layer of oxide 28, 32, 78. The entire trench is then filled with polysilicon that contacts the substrate at the bottom of the trench and is of the same dopant type as the substrate so that charge produced by the oxide layer on the sidewalls of the trench is neutralized. (See col. 4, line 56 to col. 5, line 6; and col. 5, line 64 to col. 6, line 9).

The *Kagaya* patent shows, in Fig. 1, etched trenches 9 which enclose the periphery of a FET. The patent also shows, in Fig. 26, filling an entire trench 232 with an insulator 241.

As acknowledged by the Examiner, *Yamazaki* does not teach that a lower region of the trench is filled with an electrically conducting material that is in electrical contact with the semiconductor body. The Examiner therefore contends that it would have been obvious to modify the structure of *Yamazaki* in the manner shown by *Kinney*. *Yamazaki*, however, describes that a trench filled with polysilicon is undesirable because, during subsequent thermal oxidation steps, the polysilicon expands in volume more than the surrounding silicon and exerts stress on the silicon, resulting in defects and leakage current and because the polysilicon film in the trench does not reduce parasitic capacitances. (See col. 3, line 64 to col. 4, line 13; and col. 9, lines 15-30). Thus, *Yamazaki* teaches away from filling a trench with polysilicon and cannot be combined with a reference that teaches filling a trench in this manner, such as is described by *Kinney*.

Because of the disadvantages of the polysilicon filled trench, *Yamazaki* instead teaches trench isolation using a trench filled with BPSG. The trench must be lined both at the sides and bottom with silicon oxide to prevent diffusion of dopants from the BPSG into the substrate. (See col. 11, lines 14-18). A person of ordinary skill in the relevant art, upon looking at the BPSG filled trench shown by *Yamazaki*, would therefore not look to another reference that teaches removing the bottom silicon oxide layer.

Additionally, *Kinney* shows that the entire trench is filled with polysilicon. Thus, *Kinney* merely describes the known doped-polysilicon field-shield isolation described in the Background of the Invention of the present application. (See page 2, lines 8-19). An ordinary practitioner would not find a

suggestion from the known isolation method for incorporating an oxide in the upper portion of the trench.

Moreover, as described in the present application, the known field-shield isolation is difficult to use because of the complicated wiring of the mixed field-shield regions in the regions of complimentary circuitry. A person of ordinary skill in the relevant art would not ordinarily look to use the doped-polysilicon field-shield isolation described in *Kinney* or combine it with another reference.

It follows that the Examiner has improperly combined the *Yamazaki*, *Kinney* and *Kagaya* references, and therefore claim 1 is patentably distinct and unobvious over the references.

Claims 2 and 21-26 depend from claim 1 and each further defines and limits the invention set out in the independent claims as well as calls for additional limitations. Claims 2 and 21-26 are therefore likewise patentably distinguishable over the references.

Accordingly, the withdrawal of the rejection of claims 1-2 and 21-26 under 35 U.S.C. § 103 is respectfully requested.

As it is believed that all of the rejections set forth in the Official Action have been fully met, favorable reconsideration and allowance are earnestly solicited.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he/she telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

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